A METHOD FOR FORMING A STORAGE CELL CAPACITOR COMPATIBLE WITH HIGH DIELECTRIC CONSTANT MATERIALS

The invention is a storage cell capacitor having a storage node electrode comprising a barrier layer interposed between a conductive plug and an oxidation resistant layer. A thick insulative layer protects the sidewall of the barrier layer during the deposition and anneal of a dielectric layer having a high dielectric constant.

The method comprises forming the conductive plug in a thick layer of insulative material such as oxide or oxide/nitride. The conductive plug is recessed from a planarized top surface of the thick insulative layer. The barrier layer is formed in the recess and the top surface of the barrier layer is recessed below the top surface of the oxide or oxide/nitride layer. The process continued with a formation of an oxidation resistant conductive layer and the deposition of a further oxide layer to fill remaining portions of the recess. The oxidation resistant conductive layer is planarized to expose the oxide or oxide/nitride layer and the oxide layers are then etched to expose the top surface and vertical portions of the oxidation resistant conductive layer.

Next a dielectric layer having a high dielectric constant is formed to overlie the storage node electrode and a cell plate electrode is fabricated to overlie the dielectric layer.

On page 2 before the first line please insert:

a2

--This is a continuation-in-part of co-pending application serial no. 08/390,336 filed on 2\17\1995 which is a continuation of serial no. 08/044,331 filed on 4/2/1993, now abandoned.

A continuation having docket no. 93-0320.02 of serial no. 08/313,677 filed on 9/27/1994 which is a divisional of serial no. 08/104,525 filed on 8/10/1993 and which may contain similar material is co-pending and is filed simultaneous herewith.--

On page 6, line 4 after "issues." please insert the following paragraphs:

a3

--The invention includes a storage node capacitor having a storage node electrode comprising a barrier layer interposed between a conductive plug and an oxidation resistant conductive layer and the method for fabricating the same. A thick insulative layer protects the sidewall of the barrier layer during the deposition and anneal of a dielectric layer having a high dielectric constant.

In one preferred implementation the method comprises forming the conductive plug in a thick layer of insulative material such as oxide or oxide/nitride. The conductive plug is recessed from a planarized top surface of the thick insulative layer. The barrier layer and the oxidation resistant layer are formed in the recess. A portion of the thick insulative material is removed to expose portions of the oxidation resistant layer. Remaining portions of the thick insulative material continue to encompass the barrier layer.

Next a dielectric layer having a relatively high dielectric constant is formed to overlie the storage node electrode and a cell plate electrode is then fabricated to overlie the dielectric layer. In this preferred implementation, since the barrier layer is protected during the formation of the dielectric layer by both the oxidation resistant conductive layer and the thick insulative layer there is little or no oxidation of the barrier layer or the contact plug, thereby maximizing capacitance of the storage node and reducing high contact resistance issues.

In one particular preferred embodiment, the barrier layer is tantalum or another material which experiences no oxidation during the formation of the storage cell capacitor. The oxidation resistant conductive layer is preferably a non-oxidizing conductive material such as platinum. The dielectric layer is preferably $Ba_xSr_{(1-x)}TiO_3$ [BST].

a3 Cont'd.

The insulative layer and the oxidation resistant layer protect the barrier layer from oxidizing during the deposition and anneal of the BST thereby also eliminating oxidization of the conductive plug. By minimizing or eliminating oxidization of the barrier layer and the conductive plug capacitance is maximized.--.

On page 7, line 15 after "capacitor." please insert the following paragraphs:

a4

--Figure 12 is the cross sectional view of Figure 5 following the formation of a recess in the oxide layer.

Figure 13 is the cross sectional view of Figure 12 following the deposition of a barrier layer.

Figure 14 is the cross sectional view of Figure 13 following an etch back of the barrier layer.

Figure 15 is the cross sectional view of Figure 14 following a deposition of an oxidation resistant layer.

Figure 16 is the cross sectional view of Figure 15 following a further oxide deposit and the planarization of the oxide and the oxidation resistant layer.

Figure 17 is the cross sectional view of Figure 16 following an etch back of the oxide deposits.

Figure 18 is the cross sectional view of Figure 17 following formation of a dielectric layer and cell plate layer.

Figure 19 is the cross sectional view of the capacitor made by the process described in steps 2-5 and 12-19.

Figure 20 is the cross sectional view of Figure 12 following the formation of a conductive layer.

Figure 21 is the cross sectional view of Figure 20 following removal of non silicide portions of the refractory metal (or metal nitride) layer.

Figure 22 is the cross sectional view of Figure 21 following the formation of a barrier layer.

Figure 23 is the cross sectional view of Figure 22 following an etch back of the barrier layer.

A4 cont'd.

Figure 24 is the cross sectional view of Figure 23 following a deposition of an oxidation resistant layer.

Figure 25 is the cross sectional view of Figure 24 following a further oxide deposit and the planaraiztion of the oxide and the oxidation resistant layer.

Figure 26 is the cross sectional view of Figure 25 following an etch back of the oxide deposits.

Figure 27 is the cross sectional view of Figure 26 following formation of a dielectric layer and cell plate layer.

Figure 28 is the cross sectional view of the capacitor made by the process described in steps 2-5, 12, and 20-28.--.

On page 14, line 3 after "claimed." please insert the following paragraphs:

A5

--In the crown embodiment of the invention the initial formation of the capacitor is accomplished according to the steps depicted in Figures 2-5 and described in reference to Figures 2-5. The process continues with steps 12-19. Layers corresponding to similar layers of the previous embodiments shall be numbered the same.

Referring now to Figure 12, an upper portion of each polysilicon plug 65 is removed during a dry etch in order to form recesses 70. Typically, this etch back is 50 to 400 nano meters (nm). In a case where the polysilicon plugs 65 are formed during a selective silicon growth it is possible to form the recess 70 by controlling the growth.

Referring to Figure 13, a tantalum layer 75 is formed by a chemical vapor deposition (CVD) or a sputtering process, which may be performed at room temperature. The tantalum layer 75 provides a barrier against silicon diffusion of the polysilicon plug during subsequent high temperature anneals. Other materials capable of prohibiting silicon diffusion may be used in place of tantalum such as, for example: titanium nitride, TaN, Ti, RuO_2, and Ru.

Referring to Figure 14, the tantalum layer 75 shown in Figure 7 is etched back in order to expose the oxide layer 40 and in order to retain tantalum 75 in recesses 70 overlying the polysilicon plugs 65. The tantalum layer 75 should be recessed below a top surface of the exposed oxide layer 40. The etch back may be preceded by a planarization to

a5 Contd.

remove the tantalum overlying the oxide layer 40. Portions of the oxide layer 40 may be planarized during this step. The thickness of the initial tantalum layer 75 is preferably such that after the etch back/planarization or the etch back the portion of the tantalum layer 75 retained in the recess 70 has a depth sufficient to inhibit silicon diffusion of the polysilicon plugs 65. It can be seen that at this juncture of the process only the upper surface of the tantalum layer 75 is exposed and the tantalum sidewall 80 is protected by the oxide layer 40.

Referring now to Figure 15, a platinum layer 85 is formed by CVD or a sputtering technique. The platinum layer 85 overlies the tantalum layer 75. Since the platinum layer 85 is resistant to oxidation it provides an excellent surface for the deposition of the high dielectric constant material. Other materials which are resistant to oxidation may be used in place of the platinum. For example, RuO_2 and TiN, as well as other non-oxidizing materials may be used. In this embodiment of the invention the platinum layer 85 is relatively thin, approximately 50nm thick, although other thicknesses may be used without departing from the spirit and scope of the invention. The thickness of the platinum should be great enough to substantially protect the tantalum layer 75 against oxidation during BST deposition.

In Figure 16 oxide 86 is deposited into the recess 70, and the structure is planarized to remove portions of the platinum layer 85 overlying the oxide layer 40.

In Figure 17 the oxide layers 40 and 86 have been etched to expose a vertical sidewall of the platinum layer 85 and the upper surface of the platinum layer 85. It is necessary to retain a sufficient quantity of oxide 40 at the lower sidewall of platinum layer 85 to eliminate the possibility of oxidizing the tantalum layer 75. In order to retain sufficient oxide 40 while at the same time exposing the upper surface of the platinum layer 85 the densification of the oxide 86 must be less than the densification of oxide 40 in order for the oxide layer 86 to etch at a faster rate than the oxide layer 40.

Now the fabrication of the crown embodiment the storage node electrode is complete. Although the polysilicon plug 65 is often thought of as an electrical interconnect interposed between the substrate and the storage node electrode, it can be thought of as a portion of the storage node electrode itself.

Figure 18 depicts initial formation of the storage cell capacitor following a deposition and anneal of a dielectric layer (90) overlying the platinum layer 85. The dielectric layer 90 is typified as having a high dielectric constant. The storage cell capacitor fabrication is completed with the sputter or CVD of a 50 to 200nm thick cell plate layer 95

a5 Contd.

to form a cell plate electrode. The cell plate layer 95 is typically platinum, TiN or some other conductive material.

Following the deposition of the dielectric layer 90 and the cell plate layer 95 the storage cell capacitor is patterned and the cell plate layer 95 and the dielectric layer 90 are etched to complete the fabrication of the storage cell capacitor as shown in Figure 19.

Among the suitable materials for a dielectric layer having a high dielectric constant are $Ba_xSr_{(1-x)}TiO_3$ [BST], $BaTiO_3$, $SrTiO_3$, $PbTiO_3$, $Pb(Zr,Ti)O_3$ [PZT], $(Pb,La)(Zr,Ti)O_3$ [PLZT], $(Pb,La)TiO_3$ [PLT], KNO_3, and $LiNbO_3$. In currently envisioned embodiments BST is the preferred material and is deposited at a thickness range of 30nm-300nm by RF-magnetron sputtering or CVD. The tantalum layer 75 is not oxidized during the application of a high temperature anneal due to the fact that it is protected on its sidewall by the oxide layer 40 and that it is protected on its upper surface by the platinum layer 85.

The process can be continued or modified to accommodate the steps described in U.S. patent 5,168,073, previously incorporated by reference, for providing electrical interconnection between a plurality of capacitors thus formed.

By utilizing the method of the invention, a high density memory device is provided featuring a stacked capacitor formed in a compact area as a result of a dielectric layer having a high dielectric constant. The stacked capacitor of the invention retains storage node integrity during an anneal of the dielectric layer.

In an alternate embodiment of the crown embodiment, the deposition of the tantalum layer is preceded by a deposition of a titanium barrier layer 100, see Figure 20. A thermal anneal is performed. The titanium in contact with the polysilicon plug reacts with the polysilicon to form titanium silicide during the anneal. It is possible to perform the anneal in nitrogen. In this case the titanium still reacts with the polysilicon to form titanium silicide, and the titanium which is not in contact with the polysilicon plug reacts with the nitrogen to form TiN. In addition a thin layer of nitrogen is formed overlying the titanium silicide.

In addition to titanium, other metals including refractory metals may be used. These refractory metals may include W, Co, Ta, and Mo.

Alternately a metal nitride, such as TiN, may be deposited instead of a refractory metal. The refractory metal and the metal nitride are both capable of reacting with the polysilicon plug to form a silicide during an anneal.

Fig 19

Referring now to Figure 21, the non-silicide layer (the unreacted titanium, in the case of a non-nitrogen anneal, or TiN formed during the nitrogen anneal) and the thin layer of nitrogen formed overlying the titanium silicide 105 have been removed during a wet etch. The titanium silicide 105 overlying the polysilicon plug is retained during the etch.

The process is continued as shown in Figures 22-28 and the process corresponds to the process described with respect to Figures 13-19, respectively, of the previous embodiment with the exception that the barrier layer 75 is TiN in the present embodiment rather than tantalum which was used in the previous embodiment. However, tantalum, TaN, Ti, RuO_2, and Ru may be used.

The titanium silicide layer 105 lowers a contact resistance between the polysilicon plug 65 and the TiN layer 75.

The TiN layer 75 provides a barrier against silicon diffusion of the polysilicon plug and the titanium silicide layer during subsequent high temperature anneals.

Although a process has been described for forming the storage cell capacitor, it is apparent the process is equally applicable for the fabrication of other types of capacitors used in integrated circuits. It should also be apparent to one skilled in the art that changes and modifications, such as deposition depths, may be made thereto without departing from the spirit and scope of the invention as claimed.